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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,061	02/11/2002	Donald C. Soltis JR.	10016639-1	6701

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HEWLETT-PACKARD COMPANY
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EXAMINER

PAN, DANIEL H

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)
	10/074,061	SOLTIS ET AL.
Examiner	Art Unit	
Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 11 February 2002.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-7 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1,2,4,5 and 7 is/are rejected.
 7) Claim(s) 3 and 6 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 11 February 2002 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

1. Claims 1-7 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iadonato et al. (5,371,684) in view of Clift (6,598,149) .

3. As to claim 1, Iadonato disclosed a system comprising at least :

a) calling a first group of registers (source registers);
b) detecting hazards associated with the first register identifiers (see the comparator 204 for detecting the contentions of the source registers in a given instruction in col.6, lines 63-68, col.7, lines 1-17);
c) calling a second group of registers (see the destination registers in fig.2);
d) detecting the data hazards associated with second identifiers (see col.6, lines 63-68, col.7, lines 1-17, see also the comparison of the address in col.5, lines 26-65 for background), wherein the first register identifiers [destination addresses] overlapped the first register identifiers [addresses] in the hazard detection logic (see the matching of the comparator 204 in fig.2, see also the comparison of the destination and source addresses in col.5, lines 26-65 for background).

4. Iadonato did not specifically show that his first register group and second register group crossed two or more rows as claimed. The structural relation of the architectural registers, such as the source and destination registers was not being shown. However, Clift disclosed a system including register array [10] of R0-R7 architectural registers, each of the R0-R7 occupied one row in the register file [10] (see fig.1). It would have been obvious to one of ordinary skill in the art to use Clift in Iadonato for including the two rows of the register groups as claimed because the use of Clift could provide the control ability of Iadonato to accept specific group of registers, such as rows or sub groupings of registers, in a predefined set of an integrated format, thereby reducing the hardware overheads of the storage circuit, and therefore, minimizing the latency of the access cycle, and it could be readily achieved by configuring the register file of Clift into Iadonato with modified read/write port, such that the particular row of the register file of Clift could be recognized by Iadonato in order to enhance the process in capability of Iadonato, and for the above reasons, provided a motivation.

5. As to claim 7, Iadonato also included at least :

- a) a register file [117 register file] (see fig.1);
- b) register ID file (it is ID file because it compared the addresses of the registers) for providing hazard detections (see fig.2 108) by common detection logic (see how the conflict of the source and destination registers being detected in col.6, lines 63-68, col.7, lines 1-20) .

6. As to claim 7, Iadonato did not disclose the row to row hazard detection as claimed. Iadonato disclosed register hazard detection in row to column format(see

figs. 2). However, Clift disclosed a system including register file [10] of R0-R7 architectural registers, each of the R0-R7 occupied one row in the register file [10] (see fig.1). It would have been obvious to one of ordinary skill in the art to use Clift in Iadonato for including the row to row detection as claimed because the use of Clift could provide the control ability of Iadonato to accept specific group of registers in rows in an integrated format, thereby eliminating the circuit overheads of the memory, and therefore, reducing the wait time caused by the hardware, and it could be done by configuring the register file of Clift, which taught the architectural registers were organized in rows, into Iadonato with modified read/write port, such that the particular row of the register file of Clift could be recognized by Iadonato in order to enhance the hazard detection capability of Iadonato, and in doing so, provided a motivation.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iadonato et al. (5,371,684) in view of Clift (6,598,149) as applied to claim 1 above, and further in view of Dye (6,757,807).

8. As to claim 2, neither Iadonato nor Clift specifically showed the 128-regisiter register file as claimed. However, Dye disclosed a system including a register file comprising 128 registers (e.g. see col.7, lines 47-50 [205]). It would have been obvious to one of ordinary skill in the art to use Dye in Iadonato for including the 128-register register file as claimed because the use of Dye could provide Iadonato the greater number of the storage capacity in Iadonato, and because Iadonato also disclosed the

super scalar processing (see col.1, lines 24-27), which was a suggestion of the need of more storage capacity into the register file in order to meet the super scale processing, and for the above reasons , provided a motivation.

9. Claims 4, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (5,826,055) in view of Clift (6,598,149).

10. As to claim 4, Wang disclosed at least :

- a) register file (see register file col.10, lines 1-5);
- b) an execution unit having an array of pipelines for processing instructions (see col.1, lines 45-52) and for writing bypass data in to the register file (see col.10, lines 1-5);
- c) data hazard detection logic for detecting and aliasing data hazard detection for destination and source addresses (see col.1, lines 54-54 for background, see col.6, lines 57-67).

11. Wang did not specifically show the row to row hazard detection as claimed. However, Clift disclosed a system including register file [10] of R0-R7 architectural registers, each of the R0-R7 occupied one row in the register file [10] (see fig.1). It would have been obvious to one of ordinary skill in the art to use Clift in Wang for including the row to row detection as claimed because the use of Clift could provide the control ability of Wang to adjust to different sets of registers in rows in an integrated format, therefore minimizing the circuit overheads, and reducing the latency of the memory clock, and it could be done by configuring the register file of Clift, which taught the architectural registers were organized in rows, into Wang with

modified read/write port, such that the particular row of the register file of Clift could be recognized by Wang in order to archived the improved contention determination of Wang, and therefore, provided a motivation.

12. As to claim 5, Wang also included a register ID file (see the TAG generated by RRC 204 in col.9, lines 9- 46, see the RRC 204 for facilitating the hazard detection in col.7, lines 5-24).

13. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teach the group of 32 registers identifiers to alias the data hazard detect logic to windows of 32 register frames.

14. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the mapping of the sequential 32 –registers with common hazard logic to more than 32 stacked registers of the register file to alias in 32-register sequences.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a). Fossum (4,980,817) is cited for the teaching of register file subdivided into subarrays (see col.7, lines 7-24).

b) Jacobson et al. (6,757,807) is cited for the background teaching of bypass circuit with register file (e.g. see col.2, lines 28-60).

Naffziger (6,188,633), Raje (6,105,123), Natarjan et al (5,857,104), Lesartre (5,809,275), Amerson et al (5,778,219), Hunt (5,761,490), and Shintani et al (5,721,865), Kumar et al (5,513,363) cited by applicant in page 4 of the specification have been cited in 892 attached with this Office Action.

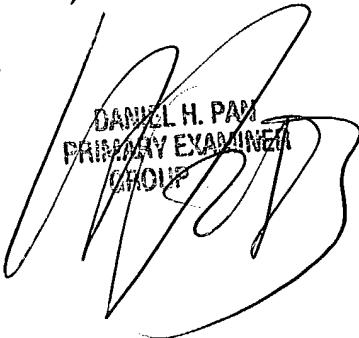
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new munber 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

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21 Century Strategic Plan


DANIEL H. PAN
PRIMARY EXAMINER
GROUP